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|---|---|
| LI, AIMEE J | |

| ART UNIT | PAPER NUMBER |
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| 2183 | |

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/972,404 | STEWART ET AL. | |
| | Examiner | Art Unit | |
| | Aimee J Li | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-20 have been considered.

### *Drawings*

2. Figures 1, 2, 3, and 4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 1, elements 26, 28, 30, and 32; Figure 3, elements 22a, 22b, 22c, and 20d; and Figure 7, element 72. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-6, 8-15, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. et al., U.S. Patent Number 5,835,746 (herein referred to

as Girardeau) in view of S. Aborhey's "Binary Decision Tree Test Function" ©1988 IEEE (herein referred to as Aborhey).

6. Referring to claim 1, Girardeau has taught a system containing:

a. An N-word sequence of single-word and double-word instructions and an instruction decoder (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3),

b. Wherein the double-word instructions comprise a marker bit pattern (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). In regards to Girardeau, there must be a marker bit pattern inherent to the instruction sequence, since there must be some way to distinguish double word instructions from singly word instructions (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

7. Girardeau has not explicitly taught wherein the instruction decoder comprises logic for implementing a binary decision tree representing every combination of single-word and double-word instructions possible for the N-word sequence and identifying each marker bit pattern combination that corresponds to a unique combination of single-

word and double-word instructions. However, Girardeau has taught a state diagram, which determines which operations are outputted based upon conditions, such as whether the instructions are single or double-word, must be implemented using some method in the controller (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). Aborhey has taught a binary decision tree has a test instruction at each node and a path traversing the nodes that leads to an output (Aborhey paragraphs 3-5). A person of ordinary skill in the art at the time the invention was made, and as stated in Aborhey, would have recognized that binary decision tree reduces the number of basic operations needed before an output is obtained (Aborhey paragraph 5), thereby increasing the speed of the processor since the number of operations needed is reduced. Therefore, a person of ordinary skill in the art at the time the invention was made would have implemented the state diagram of Girardeau via a binary tree diagram of Aborhey to increase the speed of the processor.

8. Referring to claim 2, Girardeau has taught a microprocessor, such that the instruction decoder is contained within the microprocessor and such that each unique combination of single-word and double-word instructions in the N-word sequence is executable by the microprocessor (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

9. Referring to claim 3, Girardeau has taught a memory and a cache, wherein the N-word instruction sequence is transferred from the memory to the cache in response to the microprocessor requesting a specific single-word or double-word instruction present within the N-word sequence (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

10. Referring to claim 4, Girardeau has taught wherein each word in the N-word sequence corresponds to one of a series of N consecutive memory addresses (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

11. Referring to claim 5, Girardeau has taught wherein the instruction decoder is further adapted to identify the corresponding address of at least one single-word or double-word instruction within each unique combination of single-word and double-word instructions in the N-word sequence (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

12. Referring to claim 6, Girardeau has taught wherein the instruction decoder is further adapted to identify the corresponding address of at least one single-word or double-word instruction within each unique combination of single-word and double-word instructions in the N-word sequence (Girardeau Abstract; column 1, lines 21-40; column

1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

13. Referring to claim 8, Girardeau has taught wherein the marker bit pattern is part of the op code of each double-word instruction (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). In regards to Girardeau, there must be a marker bit pattern inherent to the instruction sequence, since there must be some way to distinguish double word instructions from singly word instructions (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3) and it does not matter where the marker is held since it will function the same. See *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950).

14. Referring to claim 9, Girardeau has taught wherein the instruction decoder is implemented using standard logic cells, and shares a common semiconductor substrate with the microprocessor within an integrated circuit (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). In regards to Girardeau, sharing a common semiconductor substrate is inherent, since the device is described within one microcontroller and/or one microprocessor.

15. Referring to claim 10, Girardeau has taught a method for parsing a sequence of N words into a unique combination of single-word and double-word instructions, comprising:

a. Detecting occurrences of a marker bit pattern present in the op code of each of the double-word instructions and absent from any of the single-word instructions (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). In regards to Girardeau, there must be a marker bit pattern inherent to the instruction sequence, since there must be some way to distinguish double word instructions from singly word instructions (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3) and it does not matter where the marker is held since it will function the same. See *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950).

b. Associating with every possible N-word combination of single-word and double-word instructions a corresponding unique combination of marker bit patterns .

16. Girardeau has not explicitly taught a binary decision tree and employing the binary decision tree to determine the unique combination of single-word and double-

word instructions in the sequence of N words on the basis of the detected occurrences of marker bit patterns. However, Girardeau has taught a state diagram, which determines which operations are outputted based upon conditions, such as whether the instructions are single or double-word, must be implemented using some method in the controller (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). Aborhey has taught a binary decision tree has a test instruction at each node and a path traversing the nodes that leads to an output (Aborhey paragraphs 3-5). A person of ordinary skill in the art at the time the invention was made, and as stated in Aborhey, would have recognized that binary decision tree reduces the number of basic operations needed before an output is obtained (Aborhey paragraph 5), thereby increasing the speed of the processor since the number of operations needed is reduced. Therefore, a person of ordinary skill in the art at the time the invention was made would have implemented the state diagram of Girardeau via a binary tree diagram of Aborhey to increase the speed of the processor.

17. Referring to claim 11, Girardeau has taught employing an instruction decoder within a microprocessor to parse the sequence of N words into a unique combination of single-word and double-word instructions, wherein the microprocessor is adapted to execute said single-word and double-word instructions (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

18. Referring to claim 12, Girardeau has taught transferring the sequence of N words from a memory to a cache in response to the microprocessor requesting a specific single-word or double-word instruction present within the sequence of N words (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

19. Referring to claim 13, Girardeau has taught transferring the sequence of N words from a memory to a cache in response to the microprocessor requesting a specific single-word or double-word instruction present within the sequence of N words (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

20. Referring to claim 14, Girardeau has taught identifying the corresponding address of at least one single-word or double-word instruction within each unique combination of single-word and double-word instructions present within the sequence of N words (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

21. Referring to claim 15, Girardeau has taught identifying the corresponding address of at least one single-word or double-word instruction within each unique combination of single-word and double-word instructions present within the sequence of N words (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6;

column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

22. Referring to claim 17, Girardeau has taught including the marker bit pattern within the op code of all double-word instructions and omitting it from all single-word instructions (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). In regards to Girardeau, there must be a marker bit pattern inherent to the instruction sequence, since there must be some way to distinguish double word instructions from singly word instructions (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3) and it does not matter where the marker is held since it will function the same. See *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950).

23. Referring to claim 18, Girardeau has taught implementing the binary decision tree and marker bit pattern detection using standard logic within the microprocessor (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

24. Referring to claim 19, Girardeau has taught a memory medium, comprising:

a. An N-word sequence of single-word and double-word instructions, wherein the op-code of the double-word instructions contain a marker bit pattern (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). In regards to Girardeau, there must be a marker bit pattern inherent to the instruction sequence, since there must be some way to distinguish double word instructions from singly word instructions (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3) and it does not matter where the marker is held since it will function the same. See *In re Japikse*, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950).

b. Representing every possible combination of occurrences of the marker bit pattern for the N-word sequence, and identifying each combination associated with a unique sequence of single-word and double-word instructions (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3); and

c. Determine a unique sequence of single-word and double-word instructions based on the particular combination of occurrences of the marker bit pattern in the N-word sequence (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3).

25. Girardeau has not explicitly taught a binary decision tree. However, Girardeau has taught a state diagram, which determines which operations are outputted based upon conditions, such as whether the instructions are single or double-word, must be implemented using some method in the controller (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). Aborhey has taught a binary decision tree has a test instruction at each node and a path traversing the nodes that leads to an output (Aborhey paragraphs 3-5). A person of ordinary skill in the art at the time the invention was made, and as stated in Aborhey, would have recognized that binary decision tree reduces the number of basic operations needed before an output is obtained (Aborhey paragraph 5), thereby increasing the speed of the processor since the number of operations needed is reduced. Therefore, a person of ordinary skill in the art at the time the invention was made would have implemented the state diagram of Girardeau via a binary tree diagram of Aborhey to increase the speed of the processor.

26. Referring to claim 20, Girardeau has taught wherein the N-word sequence of single-word and double-word instructions is contained within a memory coupled to a microprocessor (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3), and wherein the microprocessor and memory occupy a monolithic substrate (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). In regards to Girardeau, sharing a common semiconductor substrate is inherent, since the device is described within one microcontroller and/or one microprocessor.

27. Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau in view of Aborhey as applied to claims 1 and 14 above, and further in view of Applicant's admitted prior art (herein referred to as Prior Art).

28. Referring to claim 7, Girardeau has taught into which single-word and double-word instructions from the N-word sequence pass in order to be executed by the microprocessor (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). Girardeau has taught not explicitly taught wherein the microprocessor further comprises a pipeline (Prior Art page 1, line 29 to page 2, line 28). However, Girardeau has taught instructions are executed in parallel (Girardeau Abstract;

column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). Prior Art has taught a pipeline (Prior Art page 1, line 28 to page 2, line 28). A person of ordinary skill in the art at the time the invention was made, and as stated in Prior Art, would have recognized that a pipeline increases the efficiency and speed of a processor (Prior Art page 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of Prior Art in the device of Girardeau to increase the efficiency and speed of the processor.

29. Referring to claim 16, Girardeau has taught after parsing the sequence of N words into a unique combination of single-word and double-word instructions (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3), placing said single-word and double-word instructions to be executed by the microprocessor (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). Girardeau has taught not explicitly taught a pipeline. However, Girardeau has taught instructions are executed in parallel (Girardeau Abstract; column 1, lines 21-40; column 1, line 52 to column 2, line 6; column 2, lines 31-35 and 44-52; column 2, line 64 to column 2, line 12; column 3, lines 28-48; column 3, lines 4-14; column 4, line 58 to column 5, line 19; Figure 2; and Figure 3). Prior Art has taught a pipeline (Prior Art page

1, line 28 to page 2, line 28). A person of ordinary skill in the art at the time the invention was made, and as stated in Prior Art, would have recognized that a pipeline increases the efficiency and speed of a processor (Prior Art page 2). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipeline of Prior Art in the device of Girardeau to increase the efficiency and speed of the processor.

***Conclusion***

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Cloke, U.S. Patent Number 4,691,254, has taught a system with single-word and double-word instructions.

b. Laurent Mauborgne's Binary Decision Graphs ©1999 have taught binary decision graphs and their uses.

c. Bernard M. E. Moret's Decision Trees and Diagrams ©1982 have taught decision trees.

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
September 14, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100